Attention!

This document has been translated from Japanese to English from its original source at:

https://github.com/hra1129/V9968_Cartridge/blob/main/fpga/V9968_Cartridge_TangNano20K/src/th9958/manual/v9968_programmers_manual_register_map.pdf

This documentation was translated on March 6, 2026, and it is important to note that it is part of a Work in Progress documentation on the development of V9968 and information could change or it can contain errors.

For the most up-to-date and accurate information, please refer to the original documentation and repository:

https://github.com/hra1129/V9968_Cartridge

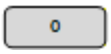
V9968 Programmer's Manual

Register Map

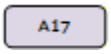
table of contents

Introduction

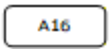
This document explains the register configuration of the V9968.



The gray bits are invalid bits. In the case of control registers, no matter what you write, nothing will happen. There are bits that were invalid in V9958 and bits that became invalid in V9968.



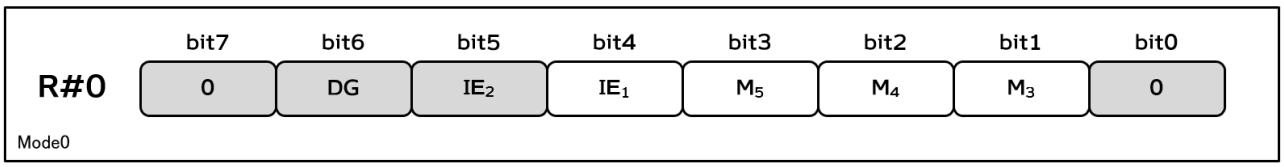
The light purple bits are bits that have been added or changed in V9968, and have some new functionality.



The white bits are bits that inherit the functions of the V9958.

Control Register

R#0 Mode0

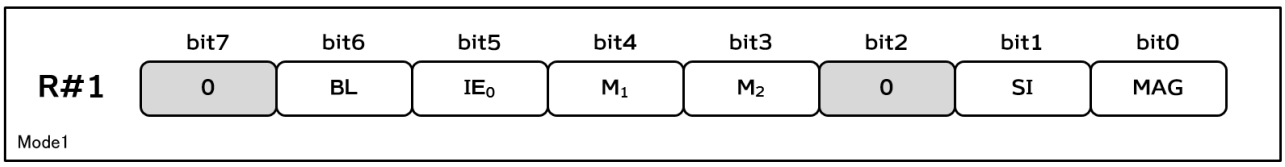


This is a mode setting register.

M5, M4, and M3 set the screen mode. These are explained together under R#1.
IE1 is the scan line interrupt enable register. Writing a 1 here will cause an interrupt to occur when the scan line specified in R#19 is displayed.
IE2 is a register used for the light pen interrupt in the V9938, but was abolished in the V9958 and is also disabled in the V9968.

DG is a register that specifies the operating mode of the VDP color bus, but is disabled in the V9968. It is not used on normal MSXs.

R#1 Mode1



This is a mode setting register.

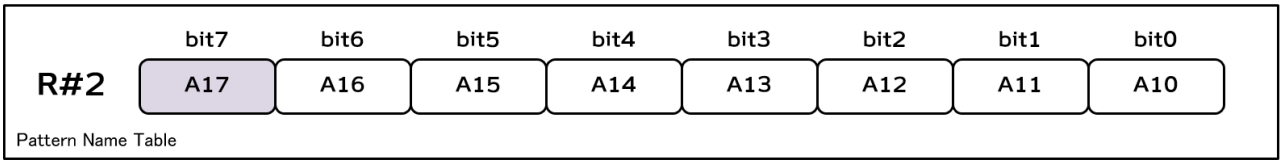
M1 and M2 set the screen mode. In conjunction with M5, M4, and M3 in R#0, various screen modes can be specified using the settings below. A list of modes is summarized below.
MAG specifies the magnification in Sprite mode 1 and Sprite mode 2. 0 is normal magnification. 1 is double the horizontal and vertical magnification. Ignored in Sprite mode 3.
SI specifies the sprite size in Sprite mode 1 and Sprite mode 2. 0 is 8 dots x 8 dots. 1 is 16 dots x 16 dots.
IE0 is the vertical synchronization interrupt enable register. Writing a 1 here will generate an interrupt at the start of the vertical blanking period.
BL is the screen display register. 0 is hidden, 1 is displayed.
When hidden, the screen will be solid with the surrounding color and no VRAM access for display will be performed. This is the fastest VDP state.

Table 1 Screen Mode Settings

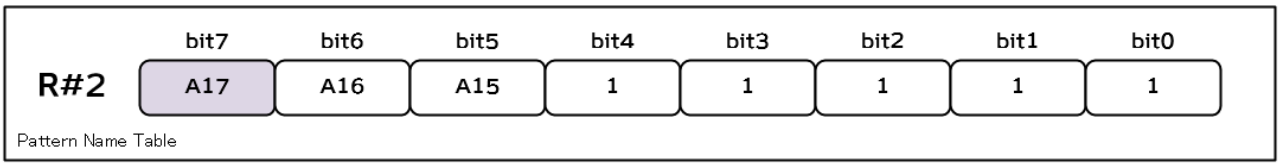
{M5,M4,M3,M2,M1}	name	MSX-BASIC mode
00000	GRAPHIC1	SCREEN1
00001	TEXT1	SCREEN0(Width40)
00010	MOSAIC	SCREEN3
00100	GRAPHIC2	SCREEN2
01000	GRAPHIC3	SCREEN4
01100	GRAPHIC4	SCREEN5

10000	GRAPHIC5	SCREEN6
10100	GRAPHIC6	SCREEN7
11100	GRAPHIC7	SCREEN8
01001	TEXT2	SCREEN0(Width80)

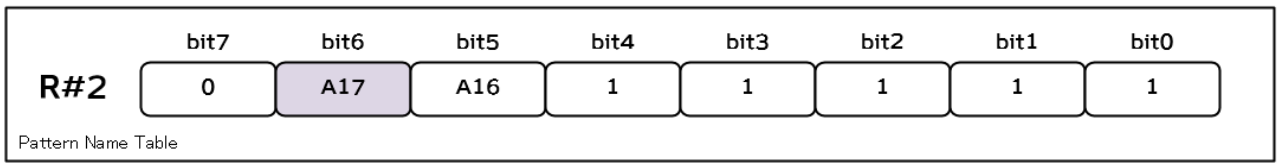
R#2 Pattern Name Table Address



Specifies the address of the pattern name table.
All bits are valid for TEXT0, TEXT1, MULTI COLOR, GRAPHIC1, GRAPHIC2, and GRAPHIC3. A17 is only valid when EVR=1 in R#20. When EVR=0, writing a 1 is the same as writing a 0.



For GRAPHIC4 and GRAPHIC5, bits 4 to 0 must be set to 1. A17 is valid only when EVR=1 in R#20. When EVR=0, writing 1 is equivalent to writing 0.

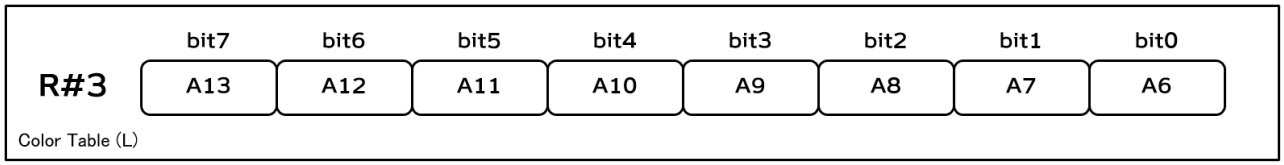


For GRAPHIC6 and GRAPHIC7, bits 4 to 0 must be set to 1; note that the bit positions are different from other modes. A17 is only valid when EVR=1 in R#20. When EVR=0, writing a 1 is the same as writing a 0.

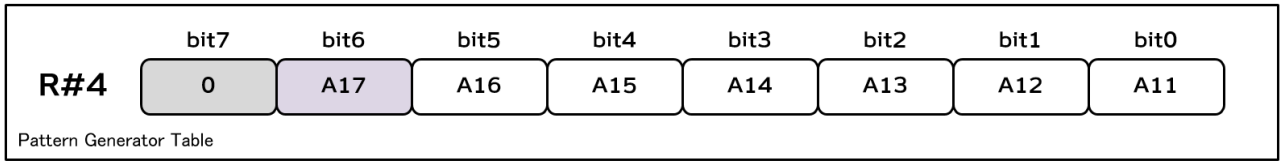
Bits set to 1 for GRAPHIC4, GRAPHIC5, GRAPHIC6, and GRAPHIC7 are mixed using an AND operation when calculating addresses internally. Therefore, setting

a 0 for a bit forces it to be fixed at 0, making it possible to display repeating patterns.
For details, see the explanation in v9968_programmers_manual_screen_mode.

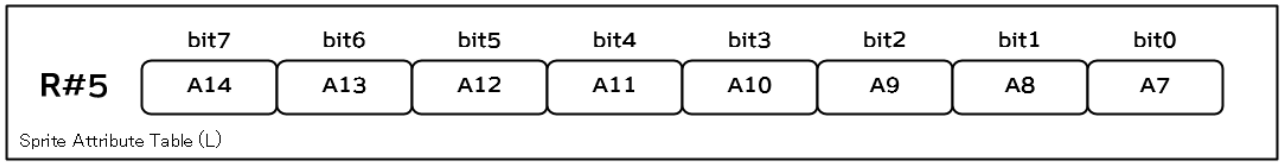
R#3 Color Table Address (L)



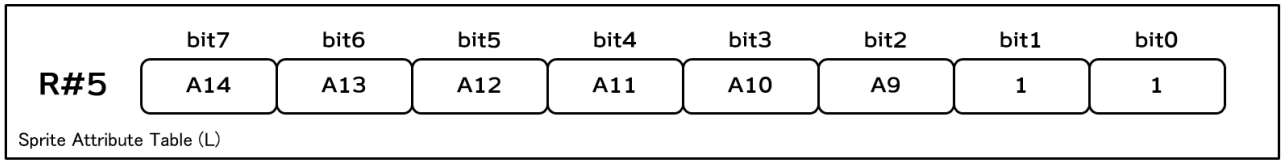
R#4 Pattern Generator Table Address



R#5 Sprite Attribute Table Address (L)

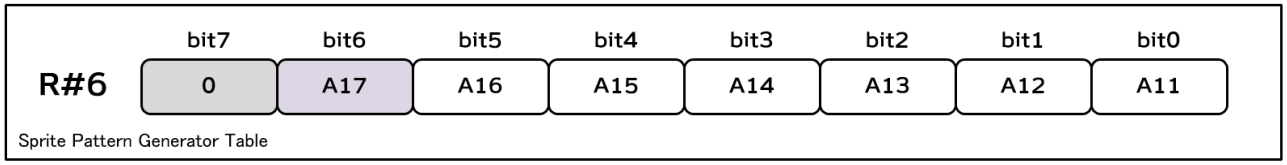


In Sprite Mode 1, specify bits 7-14 of the Sprite Attribute Table address.



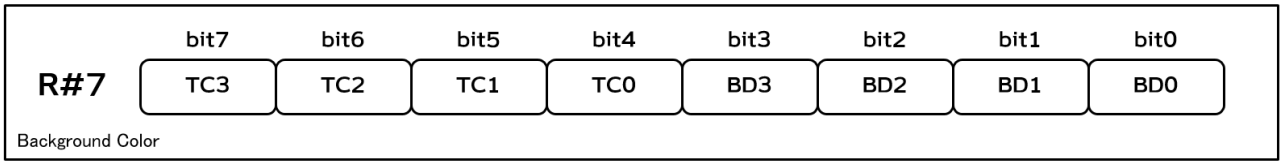
In Sprite Mode 2 and Sprite Mode 3, this specifies bits 9-14 of the Sprite Attribute Table address. R#5 bits 1 and 0 perform an AND mask on bits 8 and 7 of the Sprite Attribute Table address. Normally, this is set to 1 to prevent masking.
In Sprite Mode 2, this also serves as the Sprite Color Table address.

R#6 Sprite Pattern Generator Table Address



Specifies the address of the Sprite Pattern Generator Table that specifies the sprite shape in Sprite Modes 1 to 3. Bits 11 to 17 of the address can be specified. Bits 10 to 0 are fixed to 0.

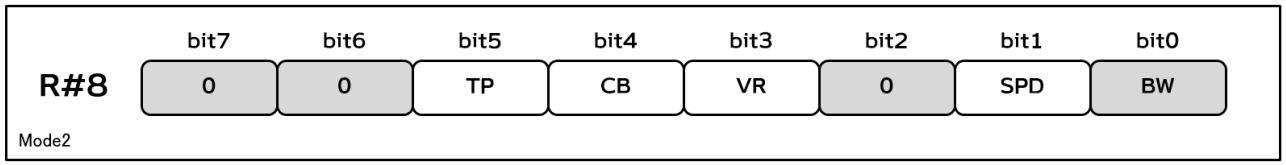
R#7 Background Color



For TEXT1 and TEXT2, bits 7-4 are the foreground color, and bits 3-0 are the background color/surround color.

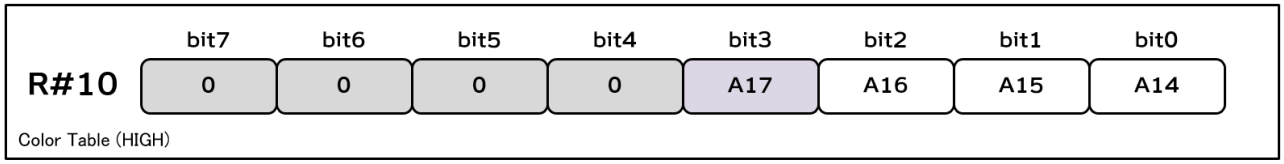
For other screen modes, bits 7-4 are invalid. Bits 3-0 are the surrounding color.

R#8 Mode2

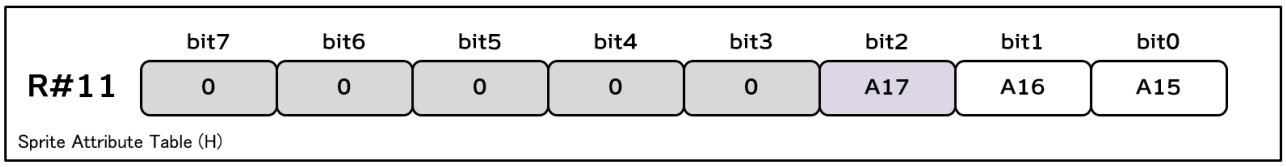


R#9 Mode3

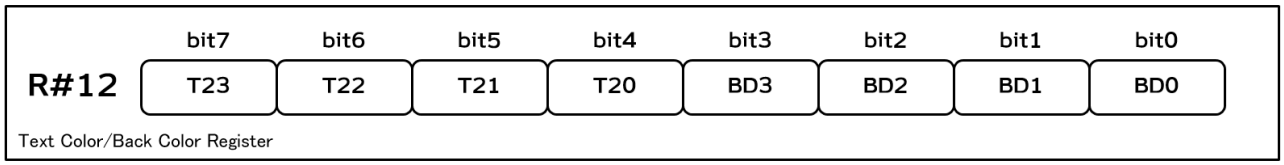
R#10 Color Table Address (H)



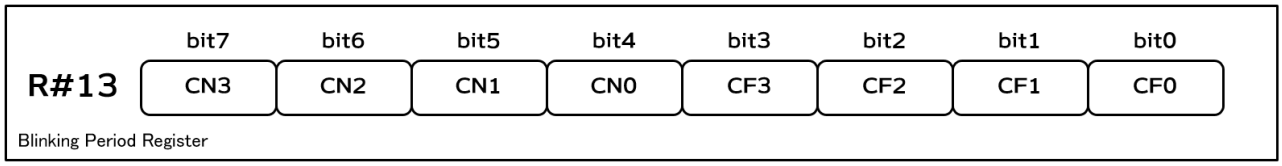
R#11 Sprite Attribute Table Address (H)



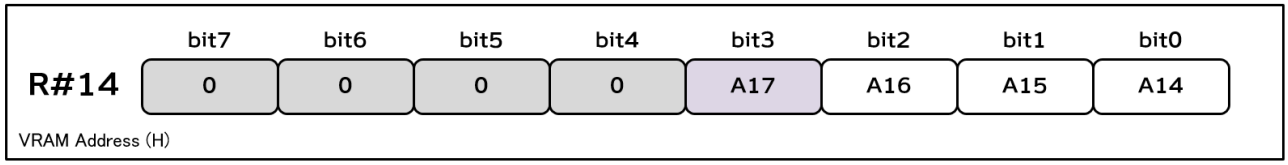
R#12 Text Color/Back Color Register



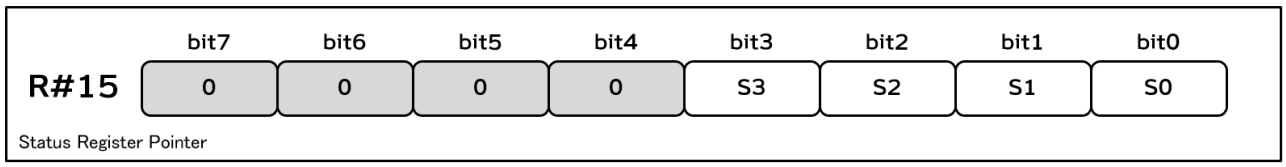
R#13 Blinking Period Register



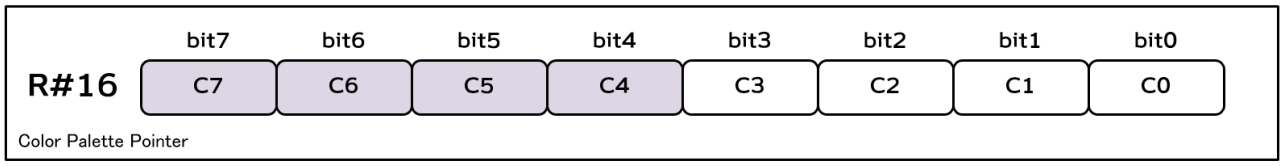
R#14 VRAM Access Base Address Register



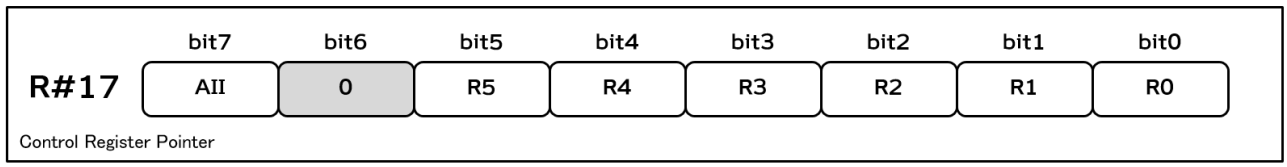
R#15 Status Register Pointer



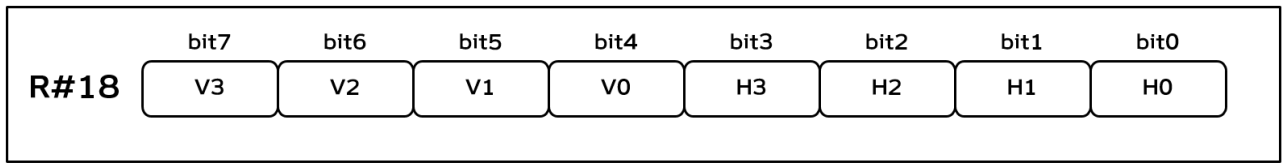
R#16 Color Palette Pointer



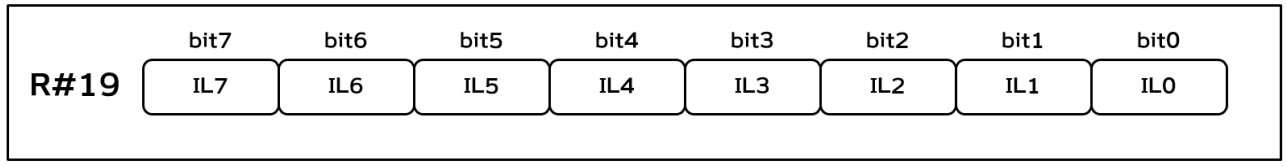
R#17 Control Register Pointer



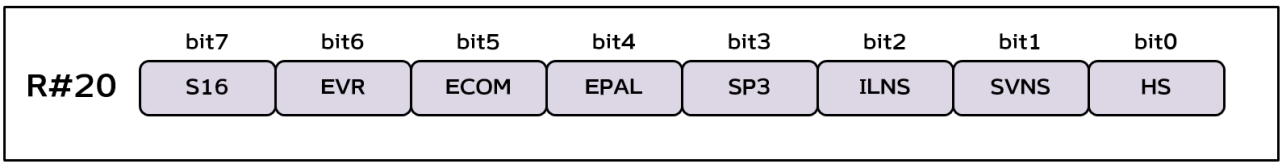
R#18 Display Adjust Register



R#19 Interrupt Line Register



R#20 Mode5



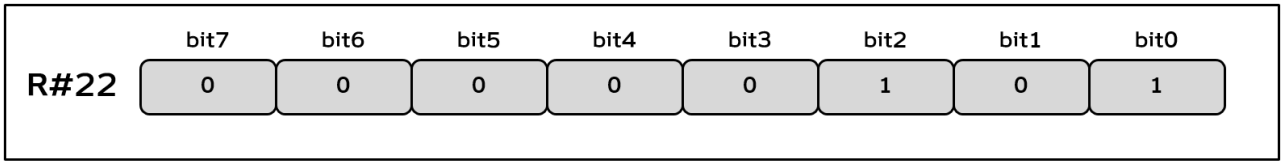
This register turns the new V9968 features on and off.
HS (High Speed command): Specifies high-speed VDP command mode. Setting it to 1 increases speed.
SVNS (Sprite Vertical position Non-following Scroll): Setting it to 1 makes the sprite unaffected by the value of R#23. Valid in all Sprite modes 1 to 3.
ILNS (Interrupt Line Non-following Scroll): Setting it to 1 makes the scan line interrupt unaffected by the value of R#23.
SP3 (Sprite mode 3): Setting it to 1 switches the sprite to Sprite mode 3.
EPAL (Expanded PALette): Setting it to 1 switches to a palette with 32,768 colors to select from.
ECOM (Expanded VDP COMmand): Setting it to 1 makes new VDP commands available.
EVR (Expanded VRAM): Expands VRAM to 256KB.
S16 (Sprite horizontal 16 planes per line mode): When set to 1 in Sprite mode 1 and 2, up to 16 sprites can be arranged horizontally. In Sprite mode 3, it is always 16.

R#21 Mode6

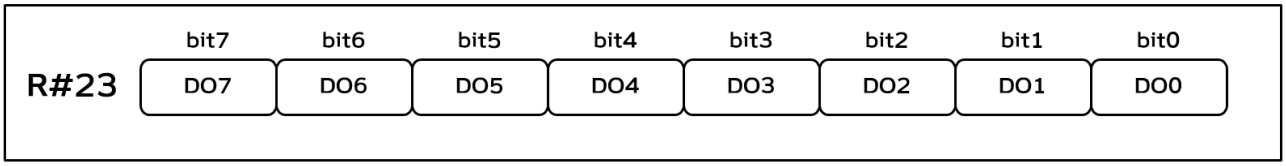
This register turns the new V9968 features on and off.
FID (FakeID): When set to 1, the VDP ID becomes V9958 (00010). The default is 1. When set to 0, the VDP ID becomes V9968 (00011). (Note: The VDP ID is S#1.)
FIL (Flat Interlace mode): When set to 1, a new interlace mode is enabled, which treats the VRAM array as a flat array when using pseudo-vertical high-

resolution interlaced display. This setting takes precedence over the setting of R#9.
CEIE (Command execute End Interrupt Enable): Enabler for the VDP command execution completion interrupt.

R#22 N/A



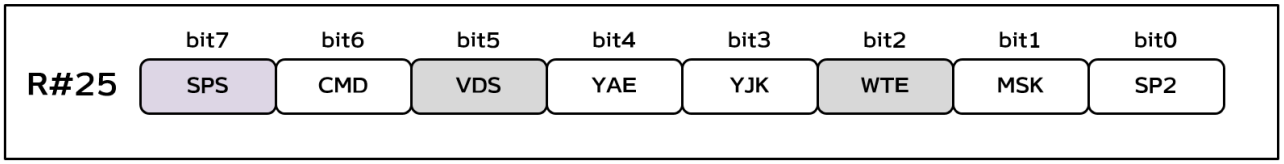
R#23 Display Offset Register



R#24 N/A

It's a missing number. It doesn't exist.

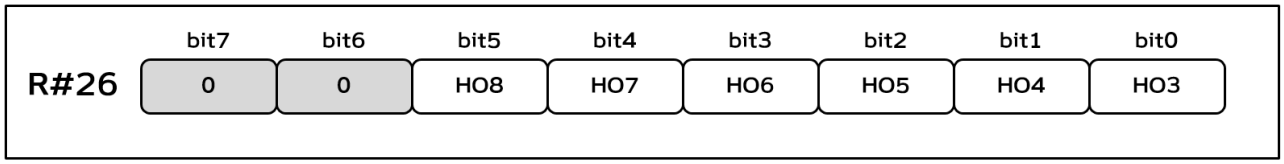
R#25 Mode4



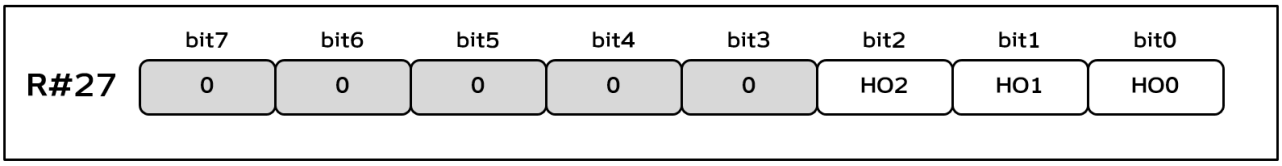
SP2:
MSK:
YJK (Y,J,K Color mode): Setting this to 1 switches to natural image mode. Requires Graphic7. Operation in other modes is not guaranteed.
YAE (Y Attribute Enable): Setting this to 1 switches to YJK+Palette hybrid mode. Requires Graphic7 and YJK=1. Operation in other modes is not guaranteed.
CMD (Command enable): Setting this to 1 enables VDP commands in non-bitmap screen modes. Operation is expected to be in Graphic7.

SPS (Sprite Priority Shuffle): Set this to 1 to enable the sprite priority shuffle function (when many sprites are lined up horizontally, they will flash instead of disappearing).

R#26 Horizontal Offset Register (By Character Units)

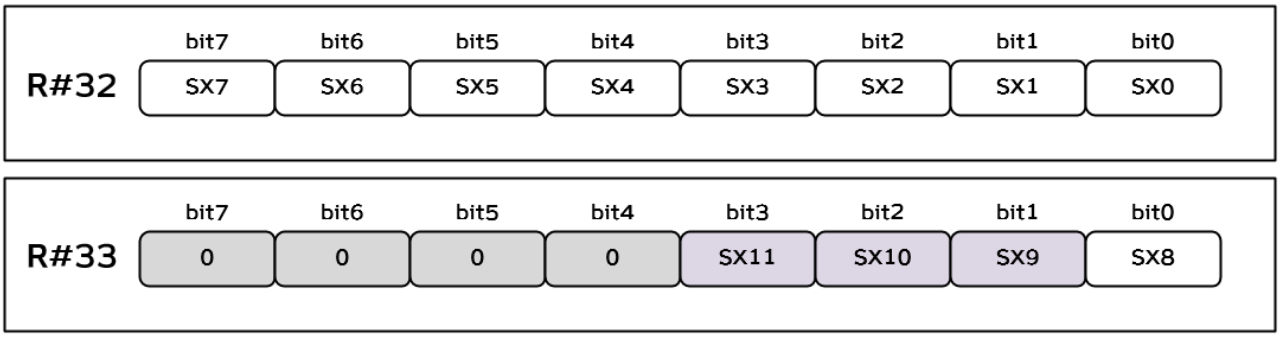


R#27 Horizontal Offset Register (By Dot Units)

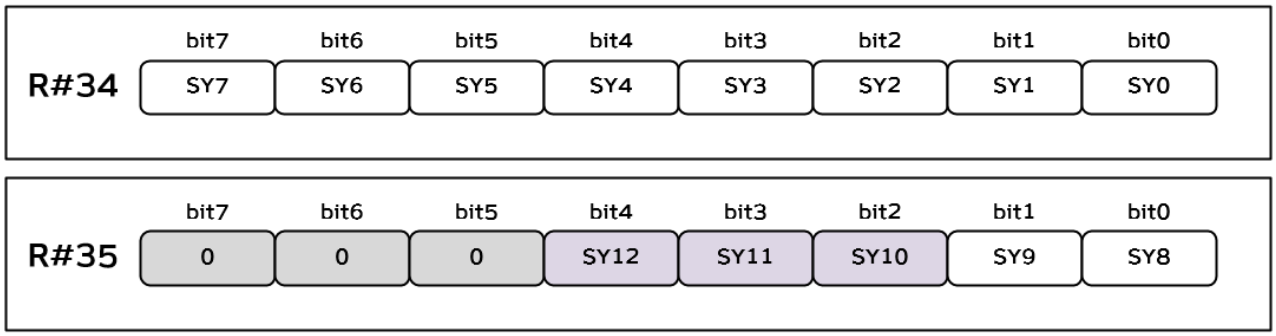


Command Register

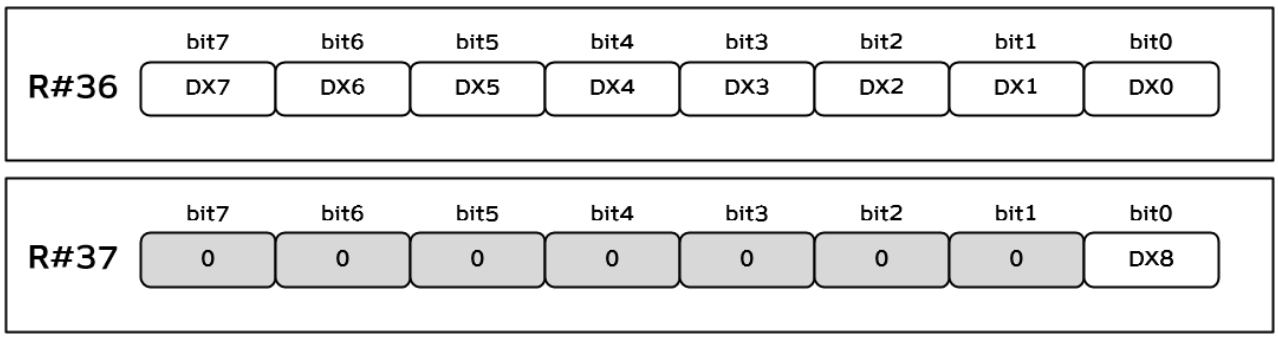
R#32, R#33 Source X Register



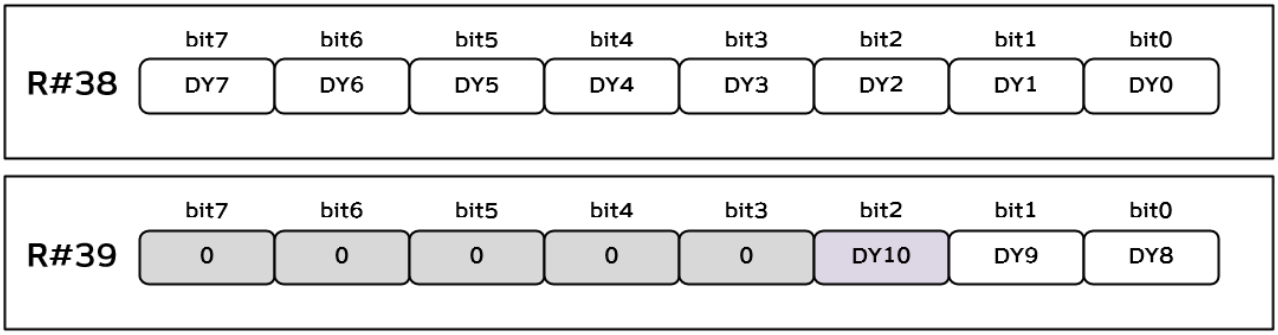
R#34, R#35 Source Y Register



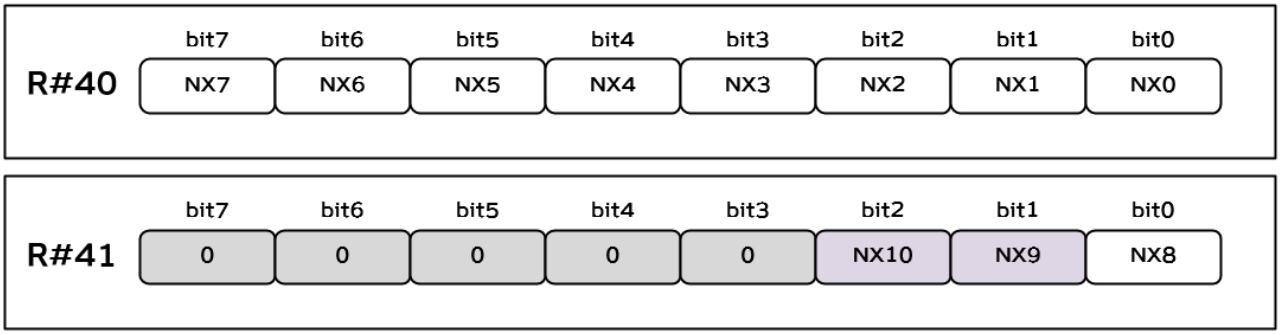
R#36, R#37 Destination X Register



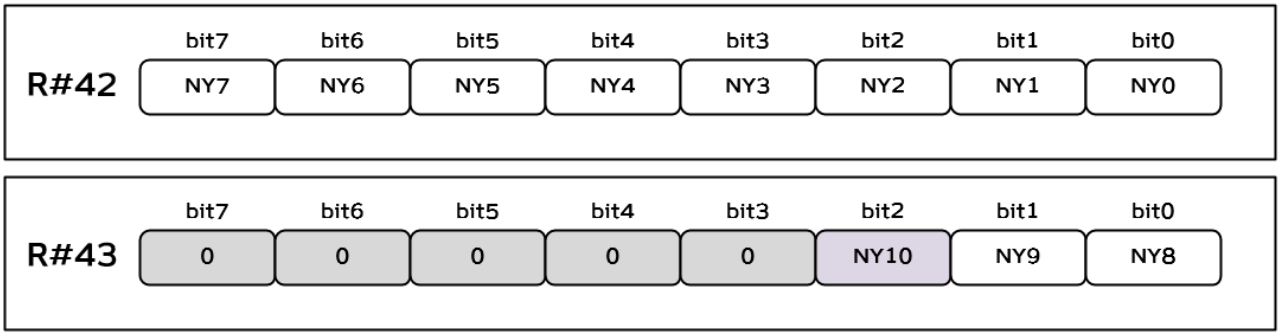
R#38, R#39 Destination Y Register



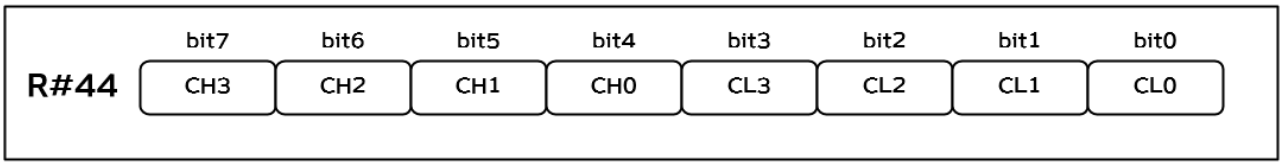
R#40, R#41 Number Of Dots X Register



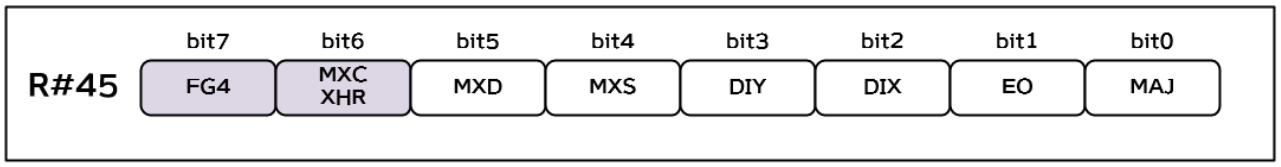
R#42, R#43 Number Of Dots Y Register



R#44 Color Register



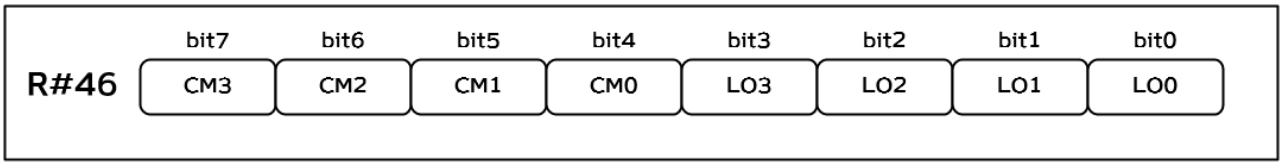
R#45 Argument Register



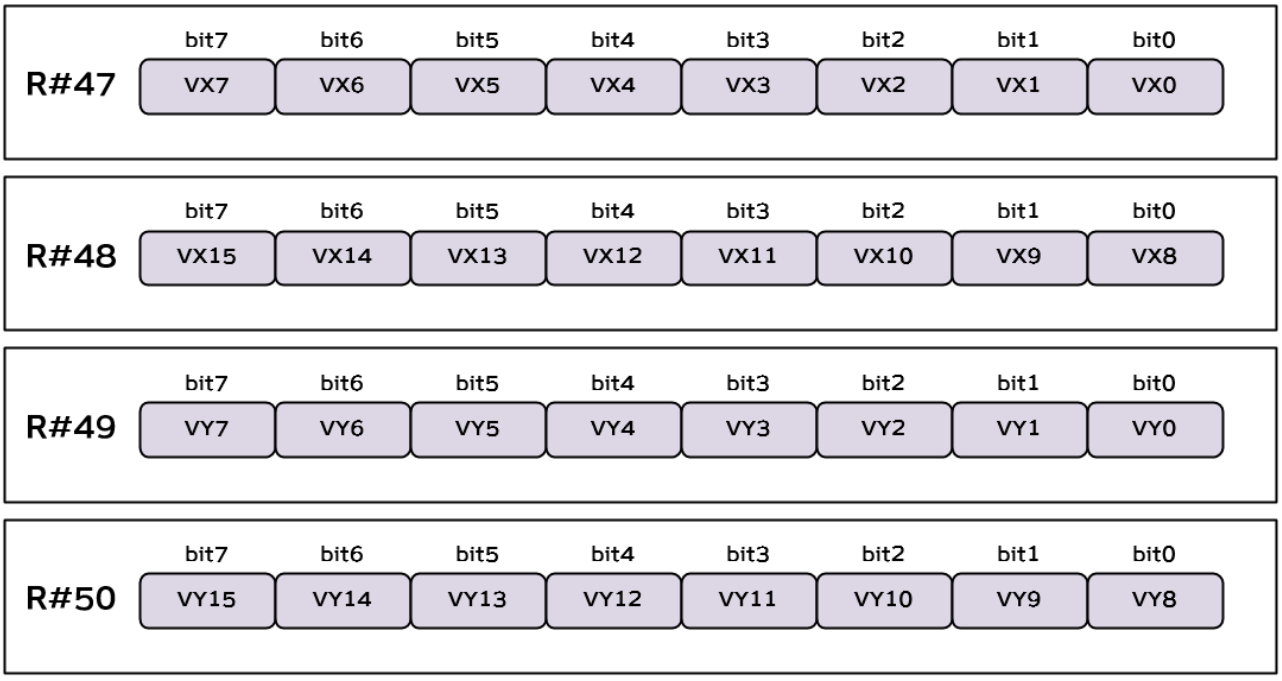
FG4 (Force Graphic4): When set to 1, the VDP command will be forced to run as Graphic4 (SCREEN5). This function is mainly used to process Sprite mode 3 patterns with the VDP command. It can be used in full-screen mode.

MXC: A dummy register for software that supports the conventional back VRAM. When set to 1, the front VRAM will be inaccessible from the CPU. The VRAM read result will be FFh. Only valid when ECOM=0.
XHR (X Half Rotate): Only valid when ECOM=1. When set to 1, the X component of the LRMM unit vector will be doubled and added. The X component of a vector rotated 90 degrees will also be doubled. This function is used to ensure consistency in vertical dot mode using Graphic5 and 6.

R#46 Command Register

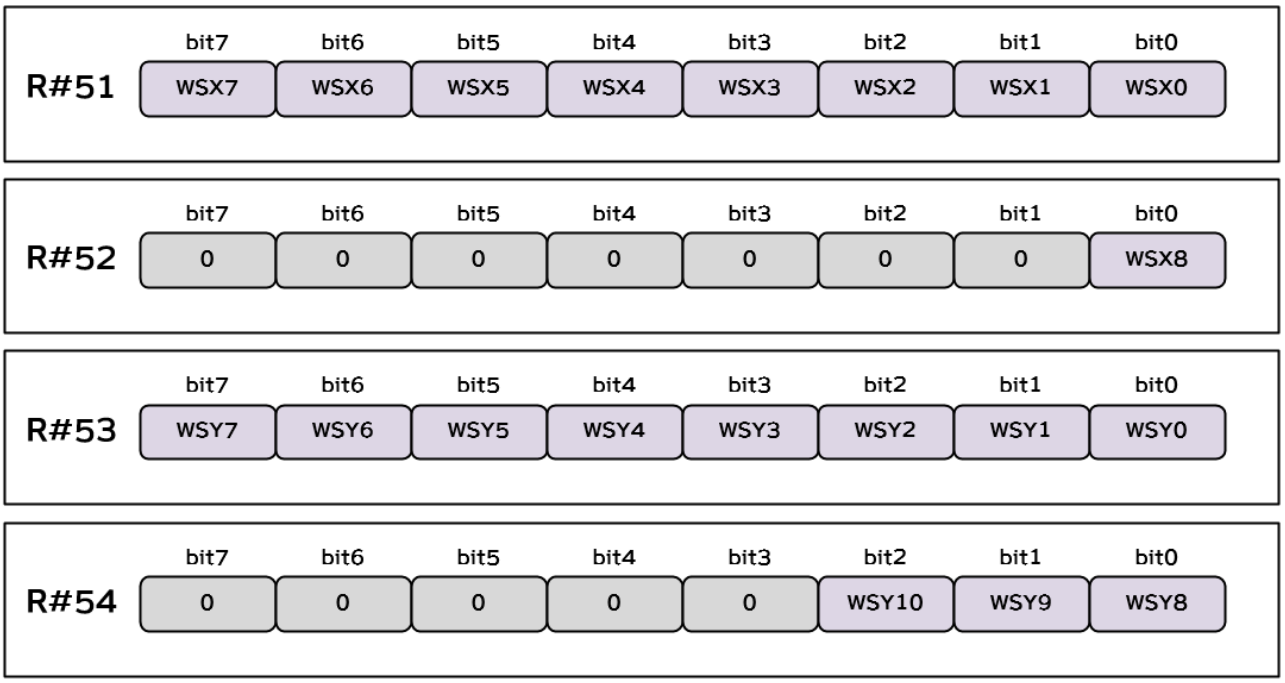


R#47, R#48, R#49, R#50 Rotation unit vector



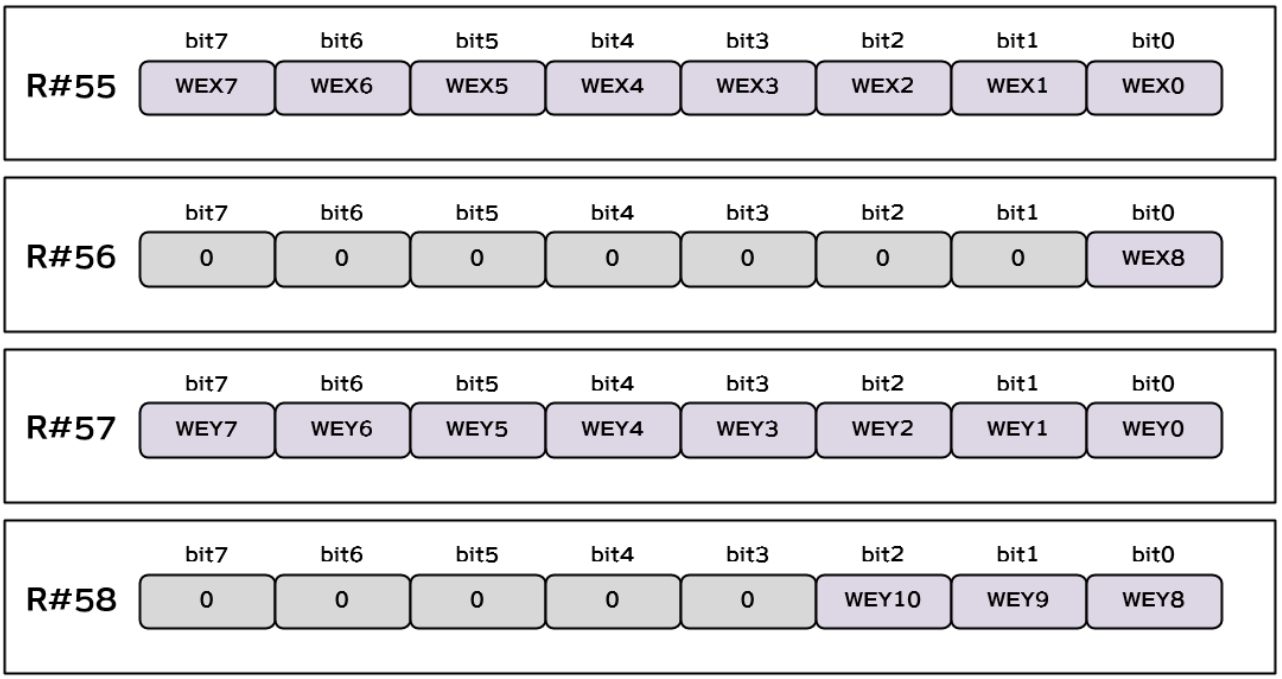
Specifies the rotation unit vector for the LRMM command. Specify as a signed fixed-point number with an 8-bit decimal part. For specific specifications, see the explanation of the LRMM command.

R#51, R#52, R#53, R#54 Output window start



Specifies the top left coordinate of the window to which the LRMM command is transferred. Only the area that fits within this window will be drawn. These coordinates themselves are considered to be inside the window. For specific specifications, see the explanation of the LRMM command.

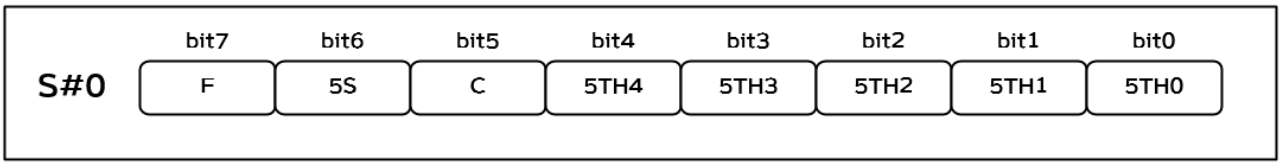
R#55, R#56, R#57, R#58 Output window end



Specifies the bottom right coordinate of the window to which the LRMM command is transferred. Only the area that fits within this window will be drawn. This coordinate itself is considered to be inside the window. For specific specifications, see the explanation of the LRMM command.

Status Register

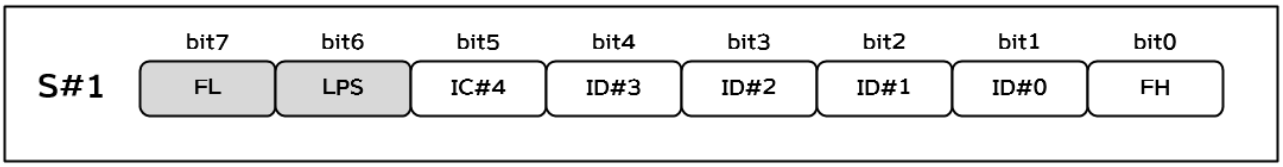
S#0 Status register 0



5TH4~0 is the sprite number that is fifth in line to disappear in Sprite mode1. In Sprite mode2, it is the sprite number that is ninth in line to disappear. In Sprite mode3, this value is invalid.
C is a flag indicating that a sprite has collided. It becomes 1 if there is a collision.

5S is a flag that indicates that there are 5 or more sprites lined up in Sprite mode 1, 9 or more in Sprite mode 2, and 17 or more in Sprite mode 3, and that some sprites are missing. If it is 1, they are lined up.
F is the vertical synchronization interrupt flag. It becomes 1 when an interrupt has occurred. It is cleared to 0 when S#0 is read.

S#1 Status register 1

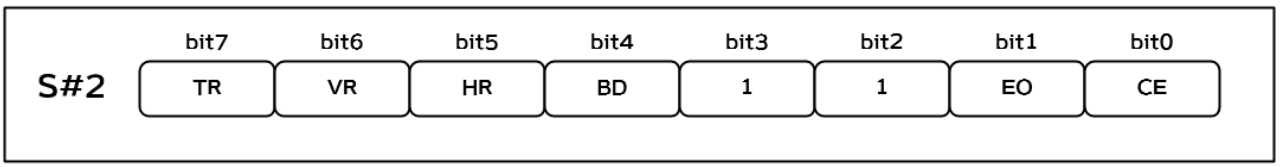


FH is set to 1 if a horizontal retrace interrupt (line interrupt, scan line interrupt) occurs, and to 0 if not. Reading S#1 clears it to 0.
ID#4 through #0 are VDP identifiers.

V9938: 00000
V9958: 00010
V9968: 00011
V9978: 00100

LPS and FL are light pen-related flags in the V9938, but were removed in the V9958 and are therefore invalid.

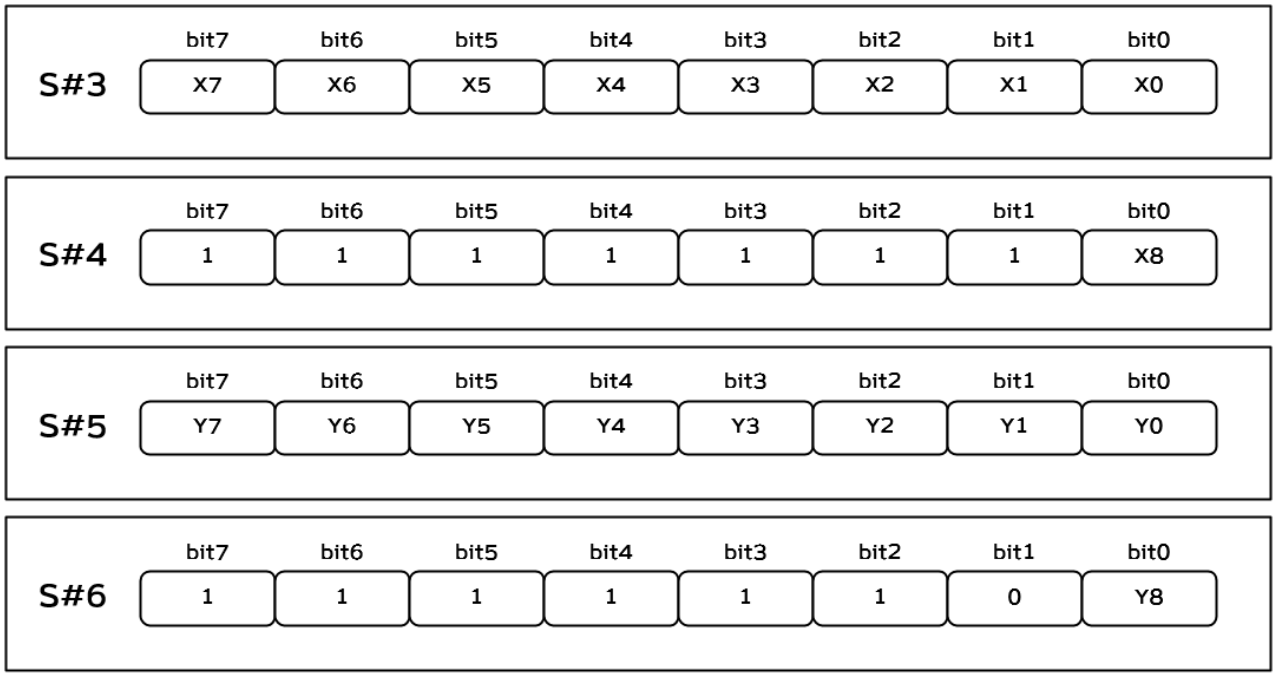
S#2 Status register 2



CE is a flag indicating whether a VDP command is in progress. It is 1 when in progress, and 0 when stopped.
EO is the even/odd field flag. It is 0 for the first field and 1 for the second field.
BD is the boundary detection flag. It is 1 if a boundary is detected by SRCH, and 0 if not. It returns to 0 when S#9 is read. For details, refer to the description of the SRCH command.
HR is a flag (negative logic) that is used during horizontal blanking. It is 0 during horizontal blanking, and 1 at all other times.

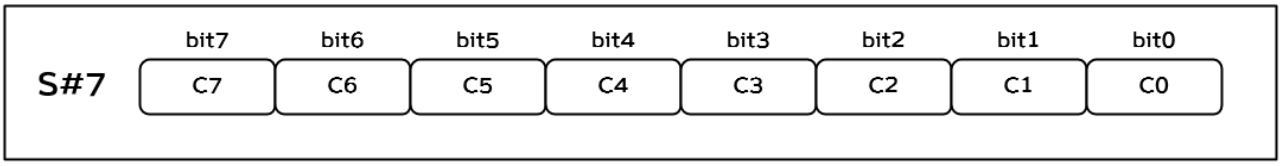
VR is a flag (negative logic) that is active during vertical blanking. It is 0 during vertical blanking, and 1 at all other times.
TR is a transfer preparation completion flag for the HMMC, LMMC, and LMCM commands. 1 means ready. 0 means not ready. For details, see the explanations for the HMMC, LMMC, and LMCM commands.

S#3, S#4, S#5, S#6 Column/Row register



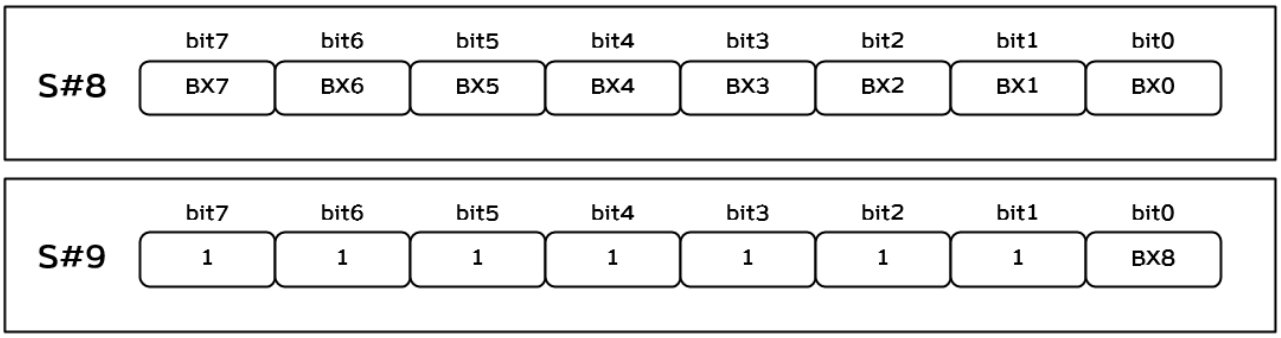
The collision coordinates of the sprite are set. See the description of sprites for details.

S#7 Color register



The pixel value read by the POINT command and LMCM command is set. For details, see the explanation of the POINT command and LMCM command.

S#8, S#9 Border X register



The X coordinate of the boundary detected by the SRCH command is set. For details, see the description of the SRCH command.